

FIG.1

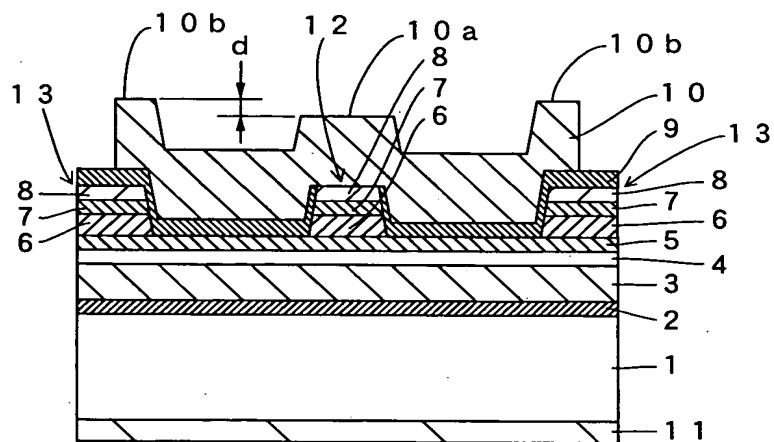


FIG.2

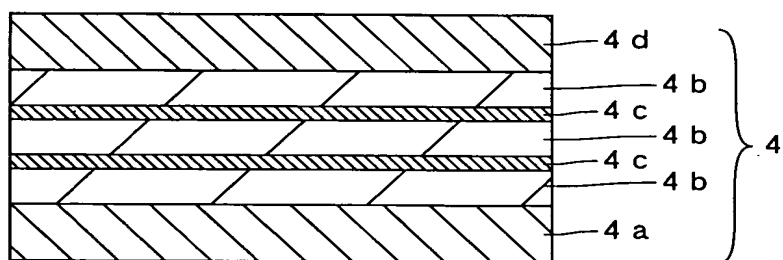


FIG.3

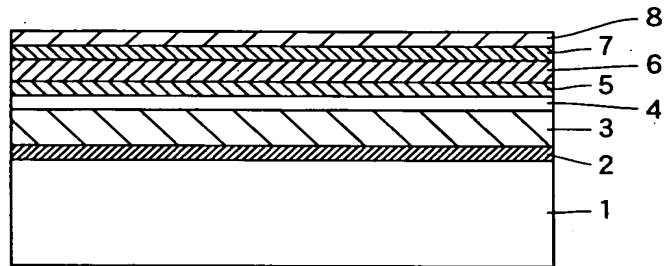


FIG.4

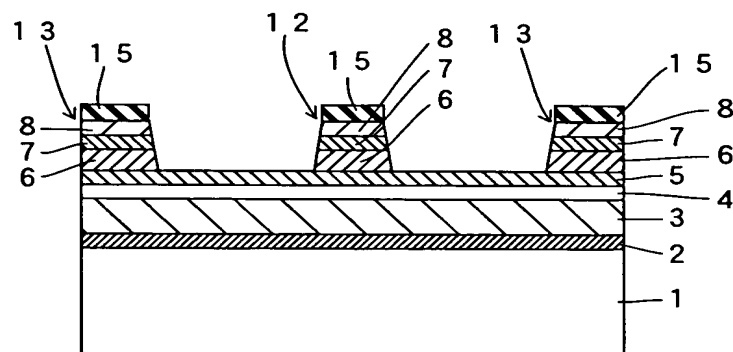


FIG.5

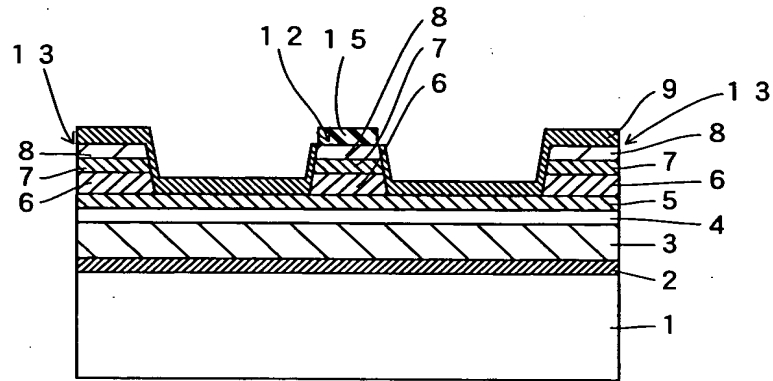


FIG.6

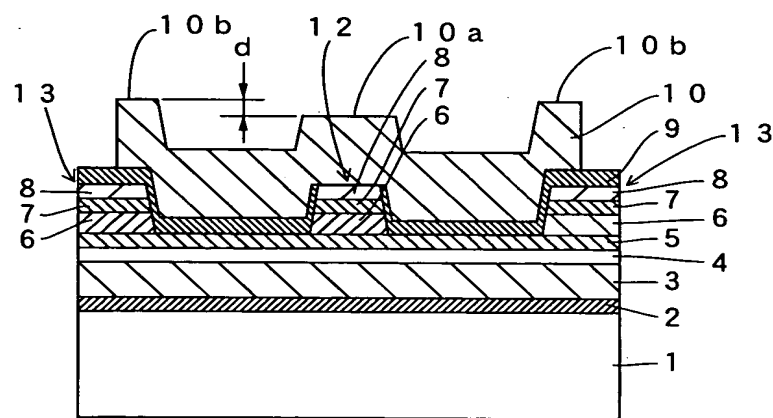


FIG.7

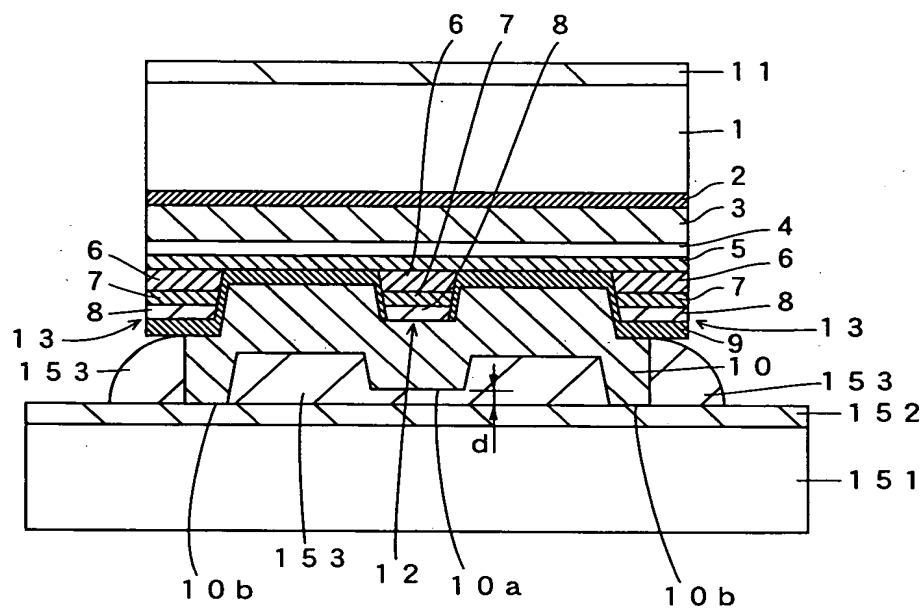


FIG.8

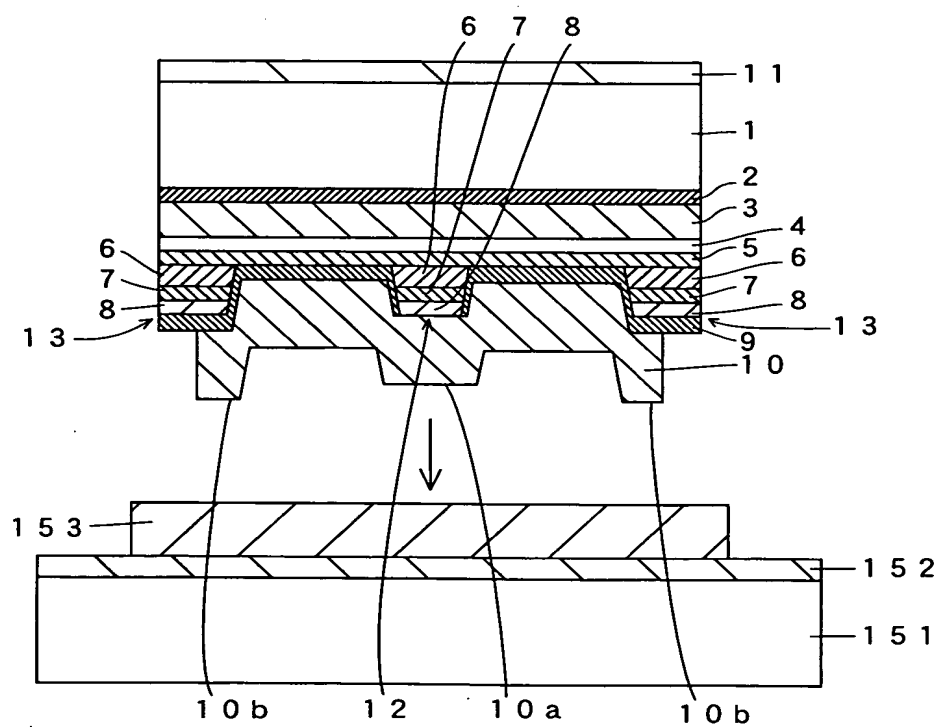


FIG.9

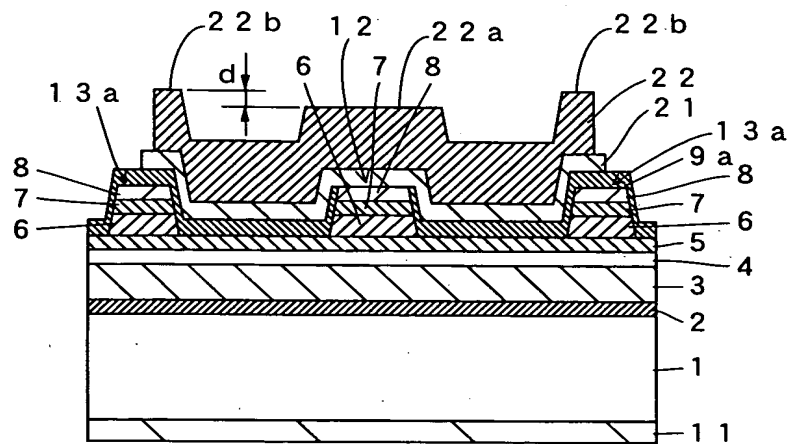


FIG.10

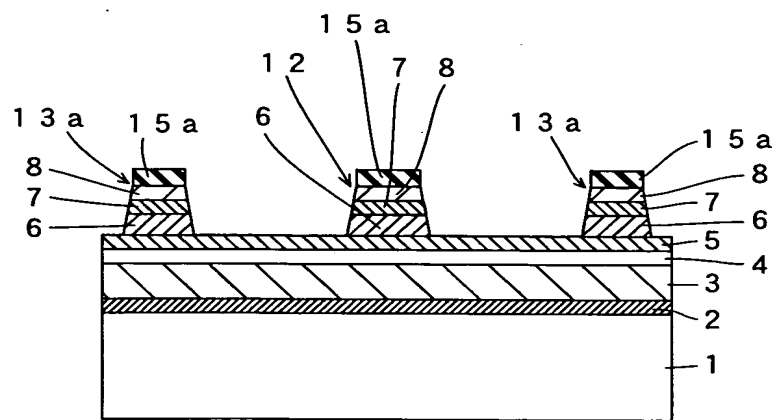


FIG.11

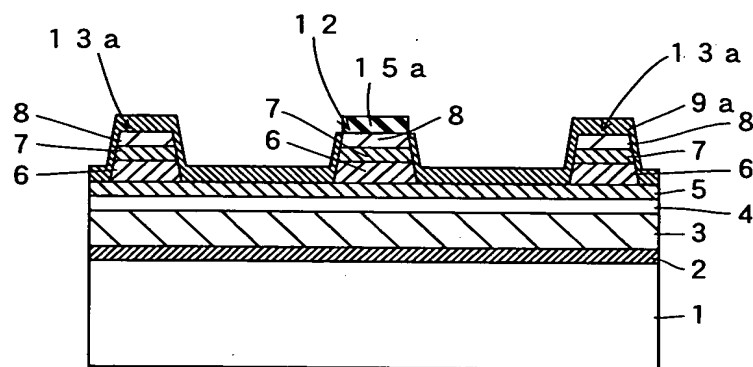


FIG.12

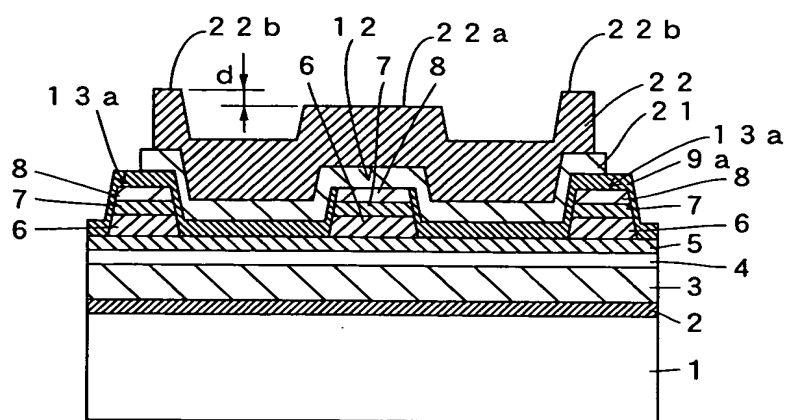


FIG.13

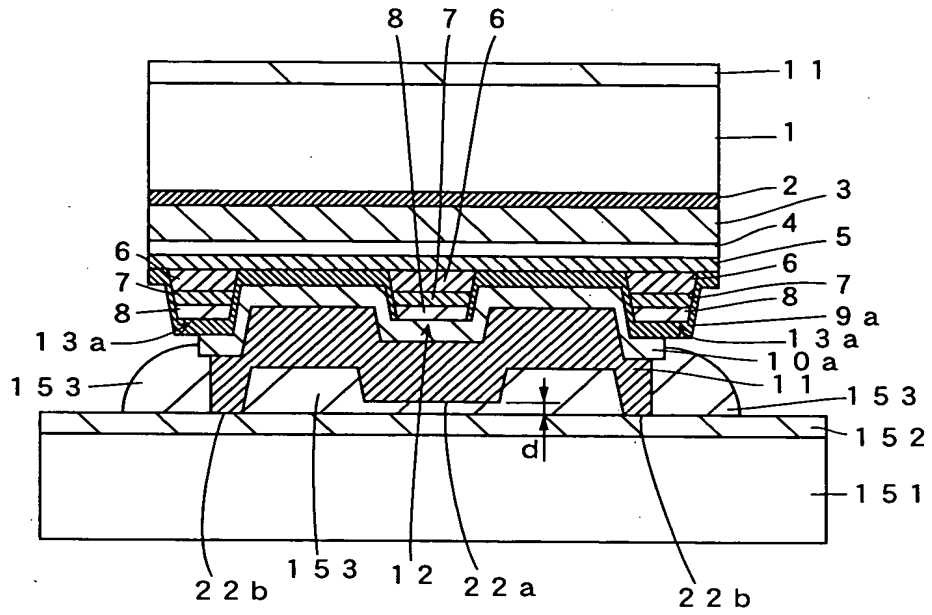


FIG.14

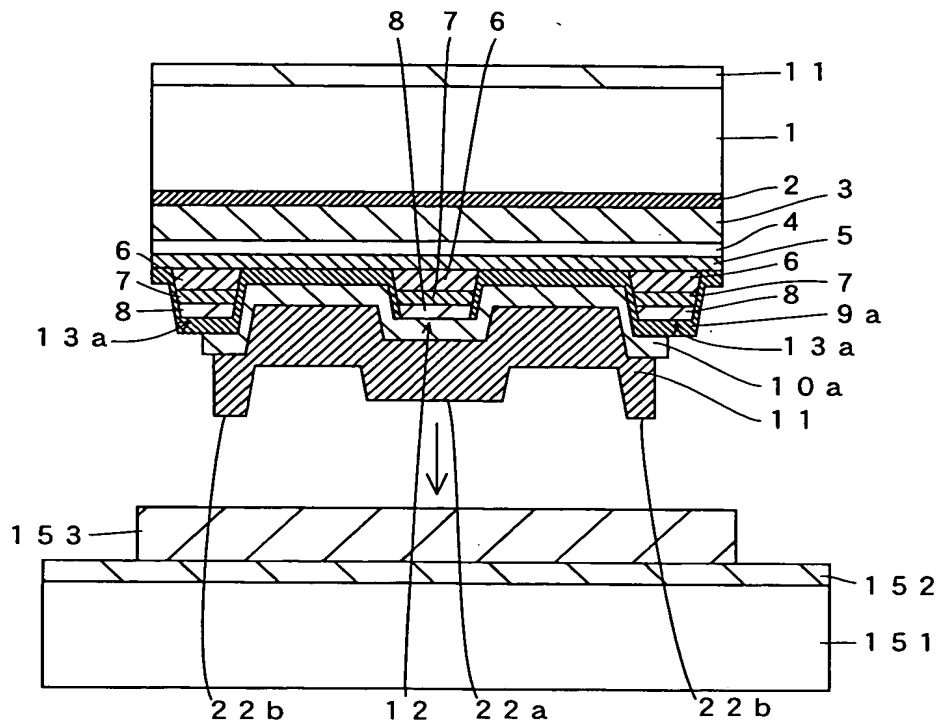


FIG.15

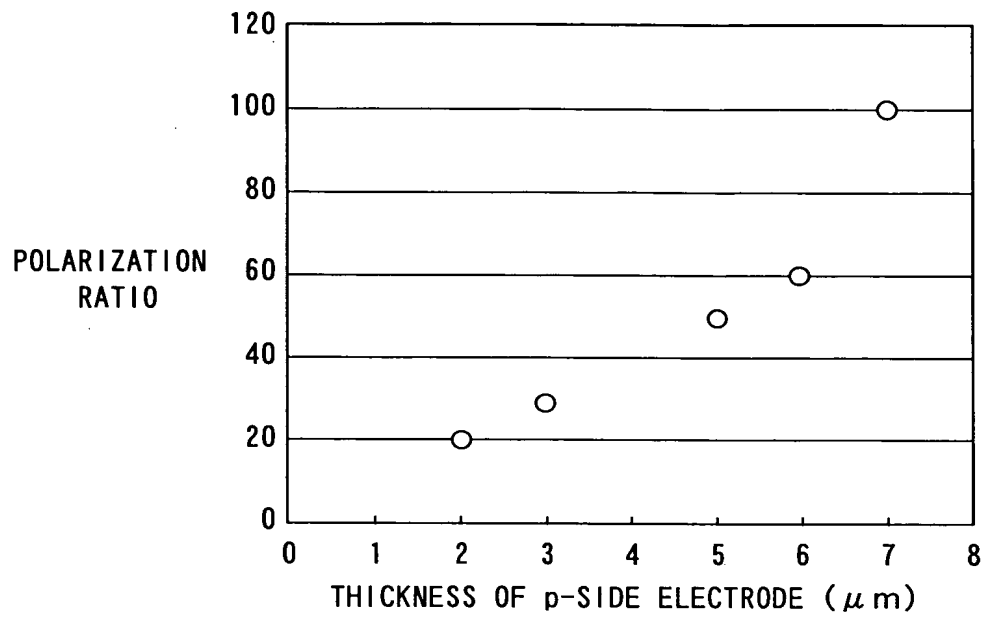


FIG.16

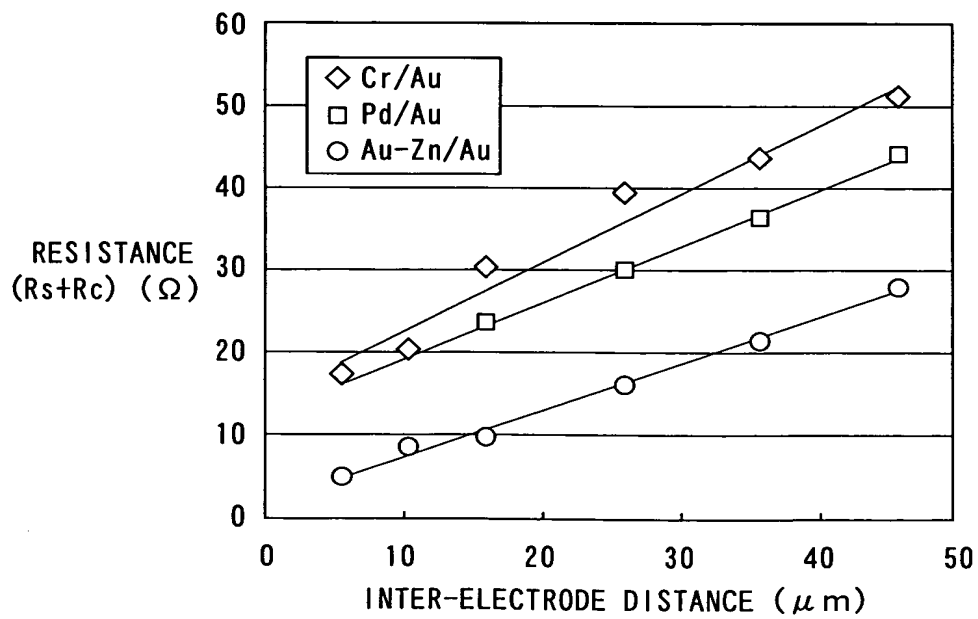


FIG.17

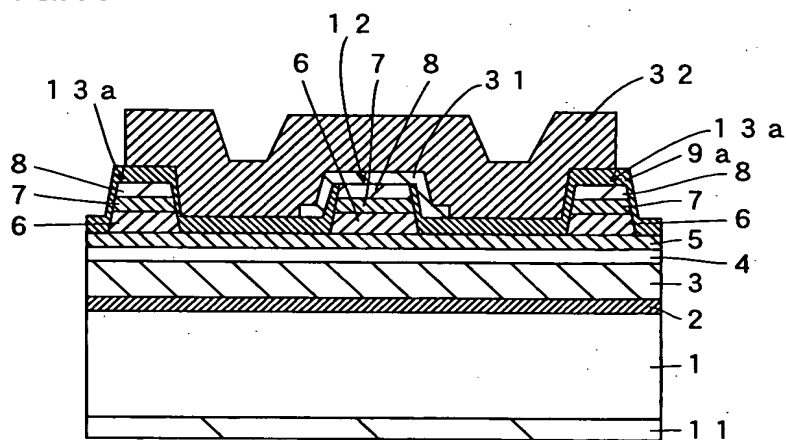


FIG.18

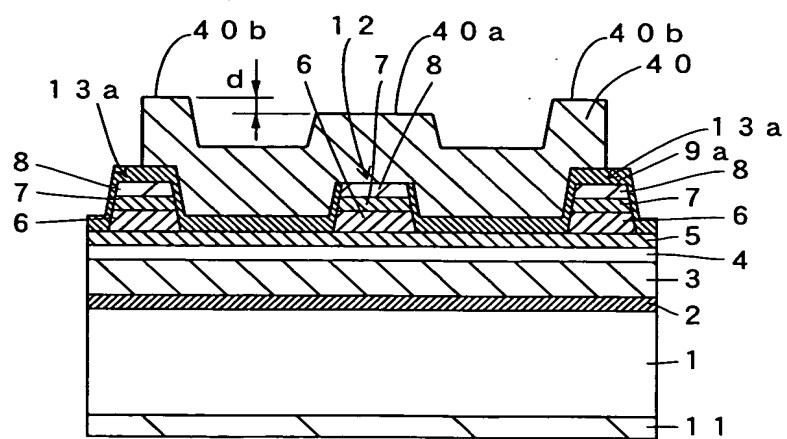


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 151 with a layer 153. A central region 12 is surrounded by a layer 40. A top layer 11 is shown. Various other layers and structures are labeled with numbers 1 through 15.

FIG.21

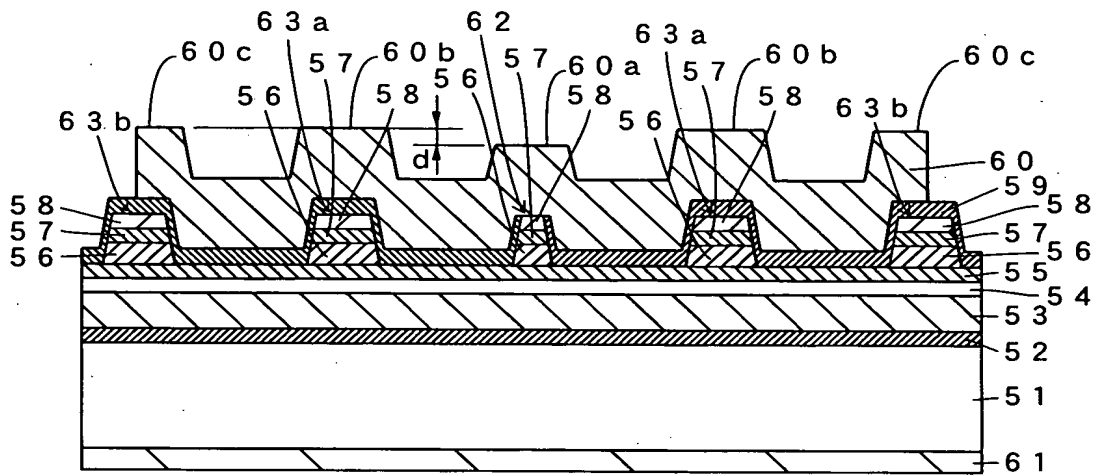


FIG.22

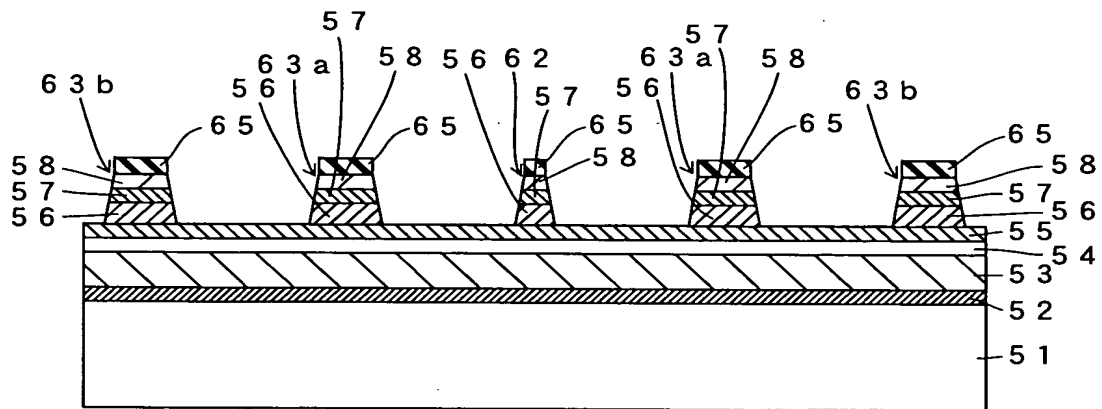


FIG.23

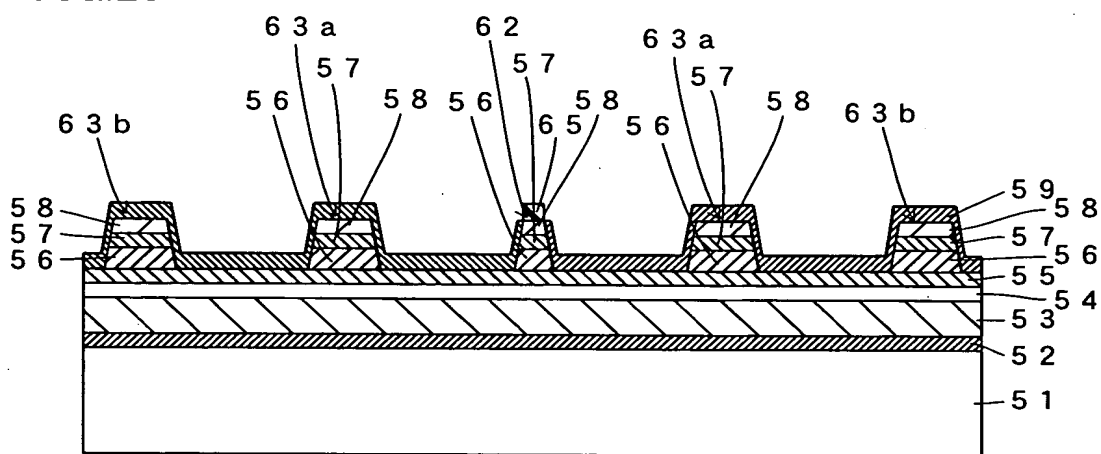


FIG.24

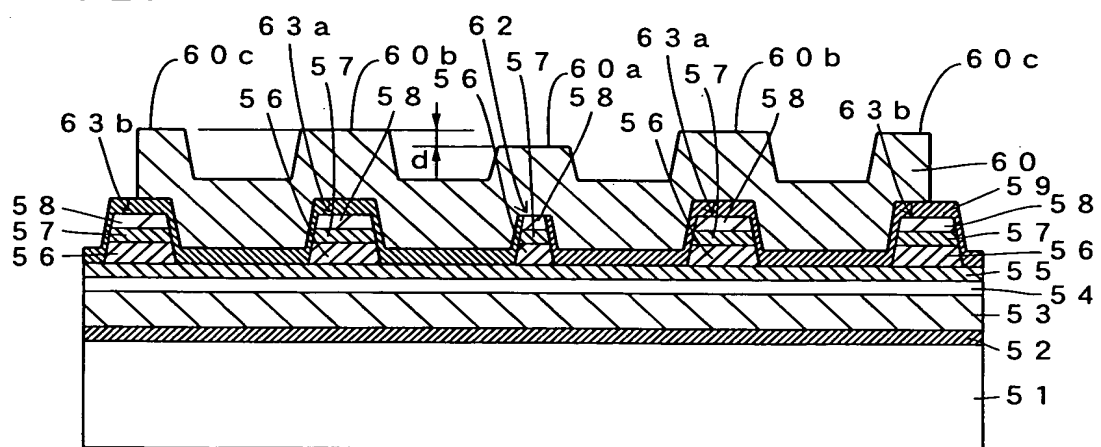






FIG.29

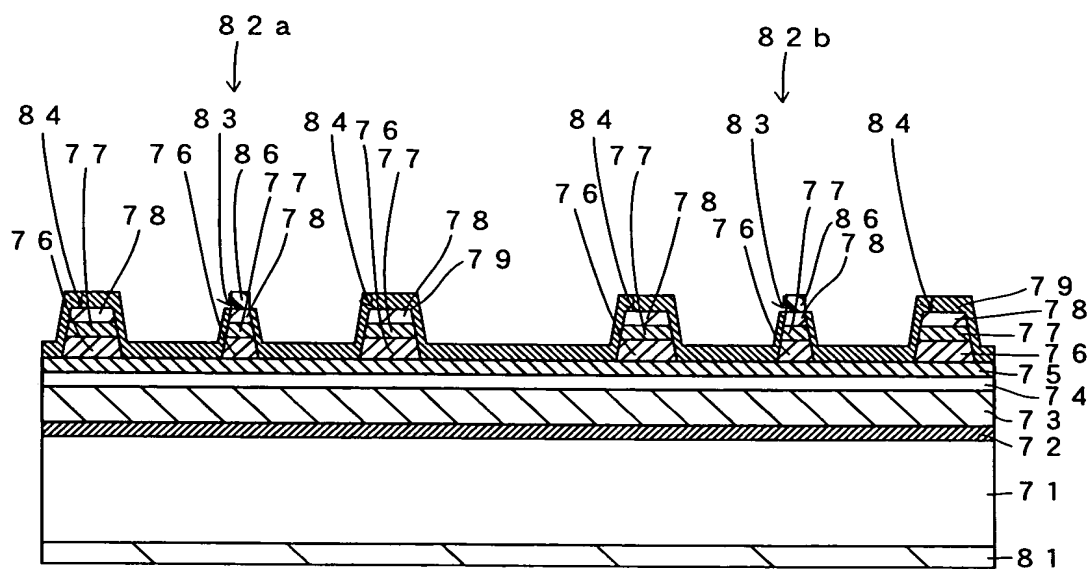


FIG.30

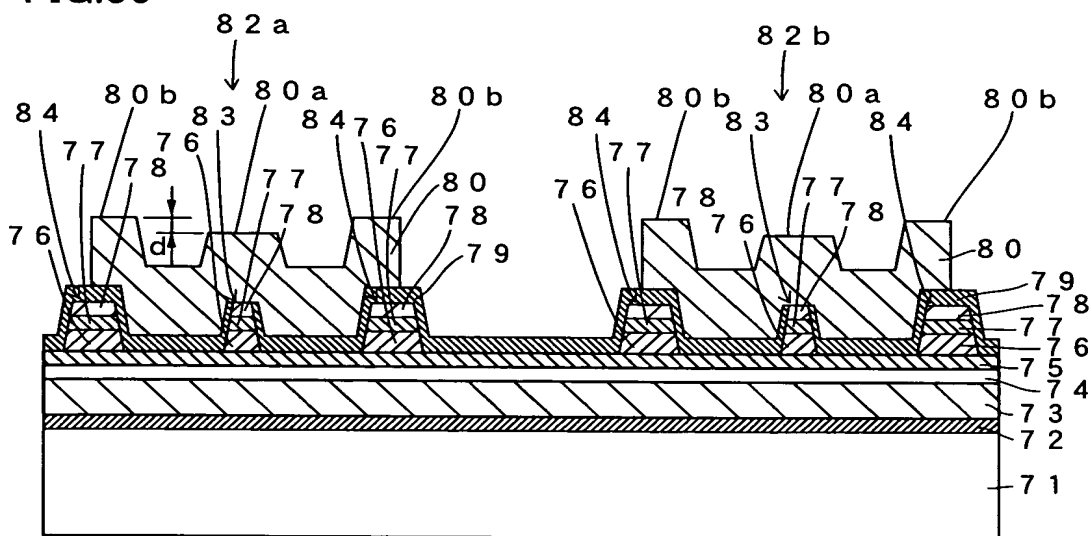


FIG.31

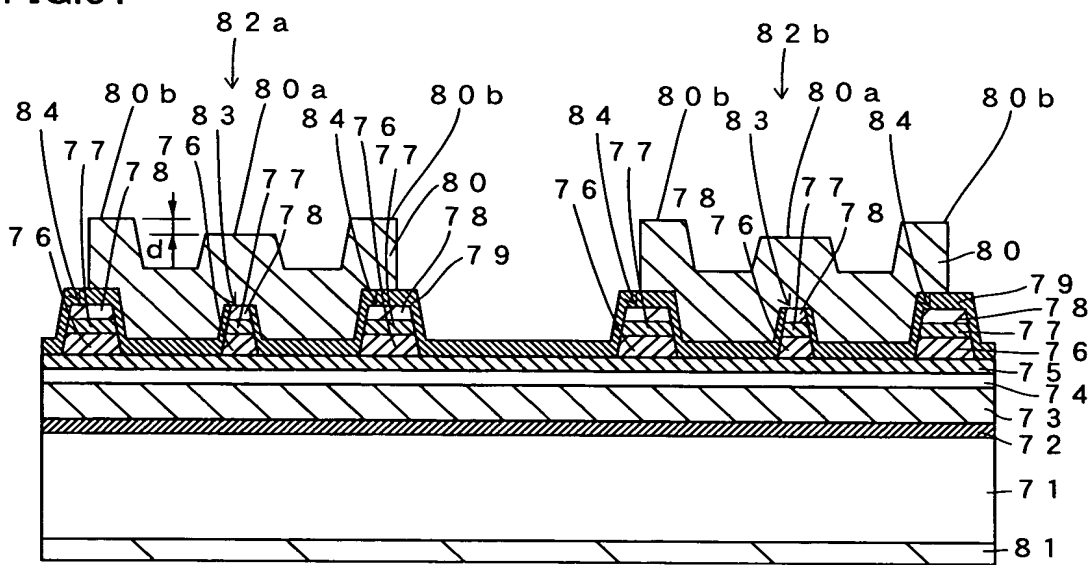


FIG.32

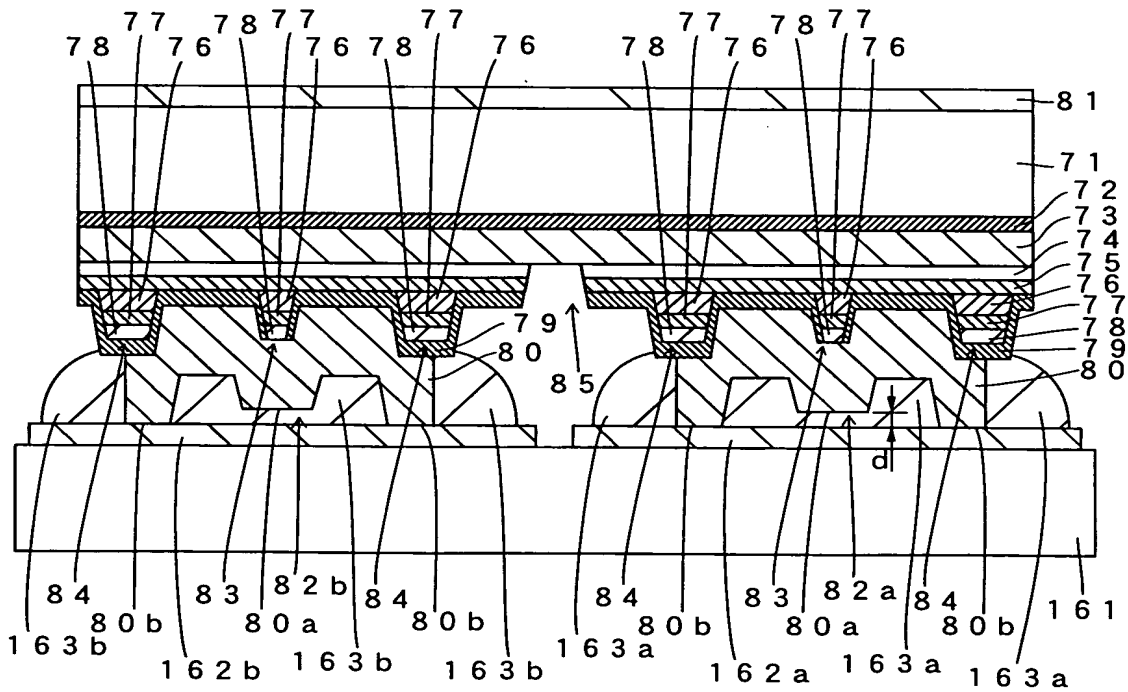


FIG.33

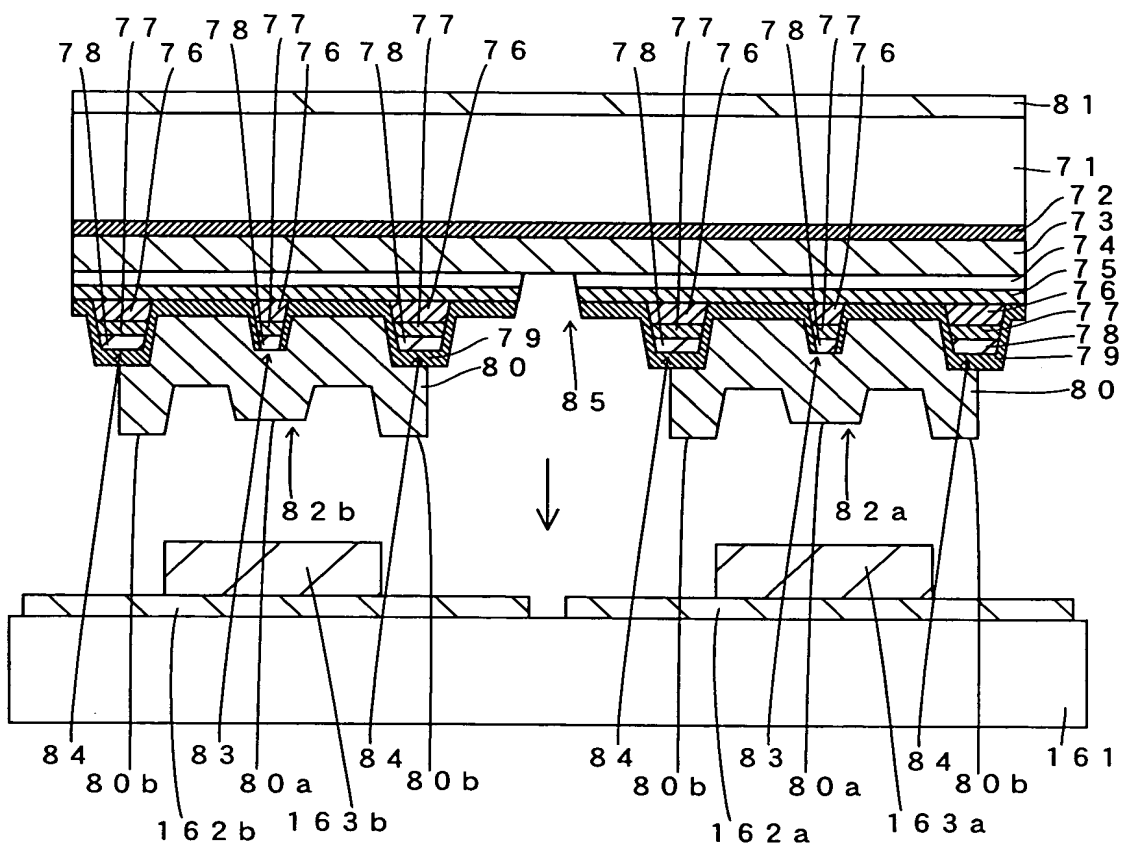


FIG.34

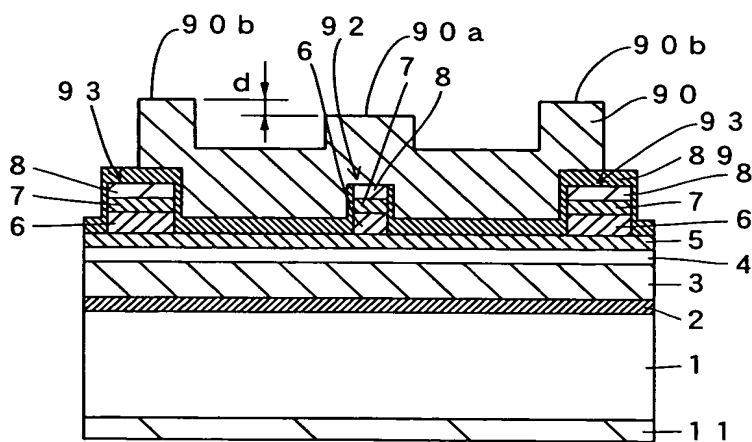


FIG.35

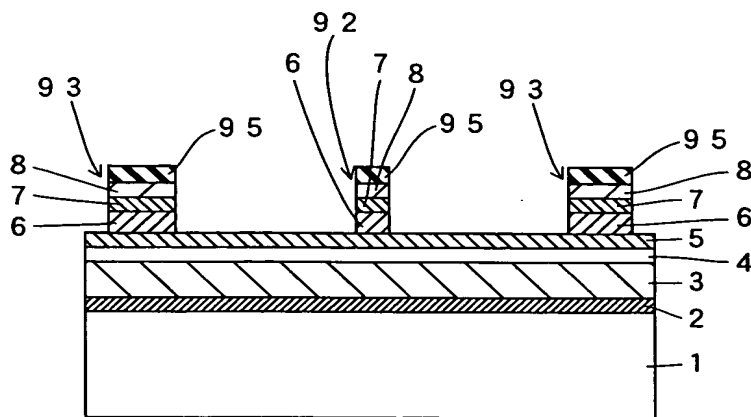


FIG.36

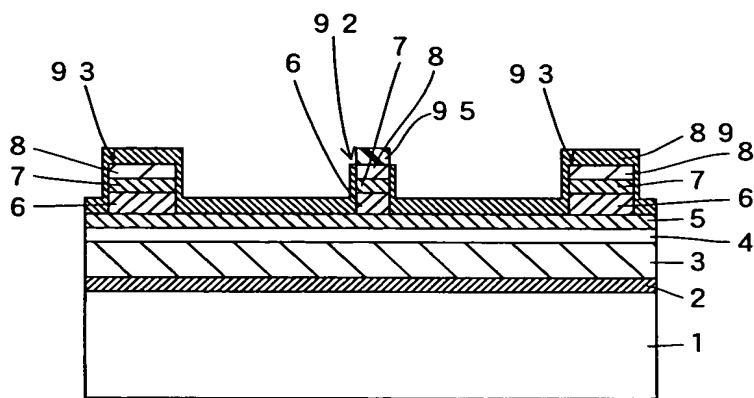


FIG.37

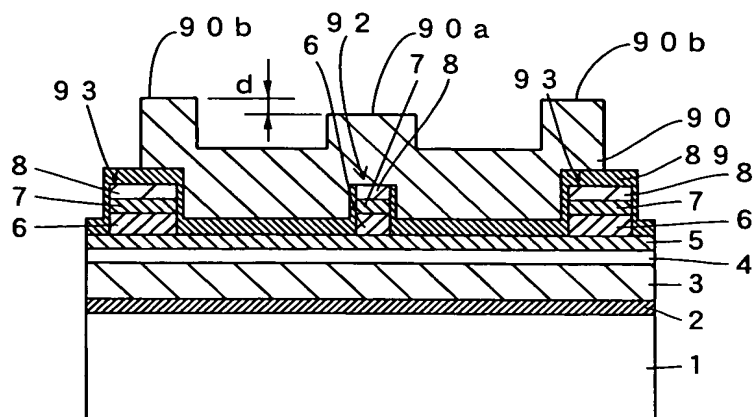


FIG.38

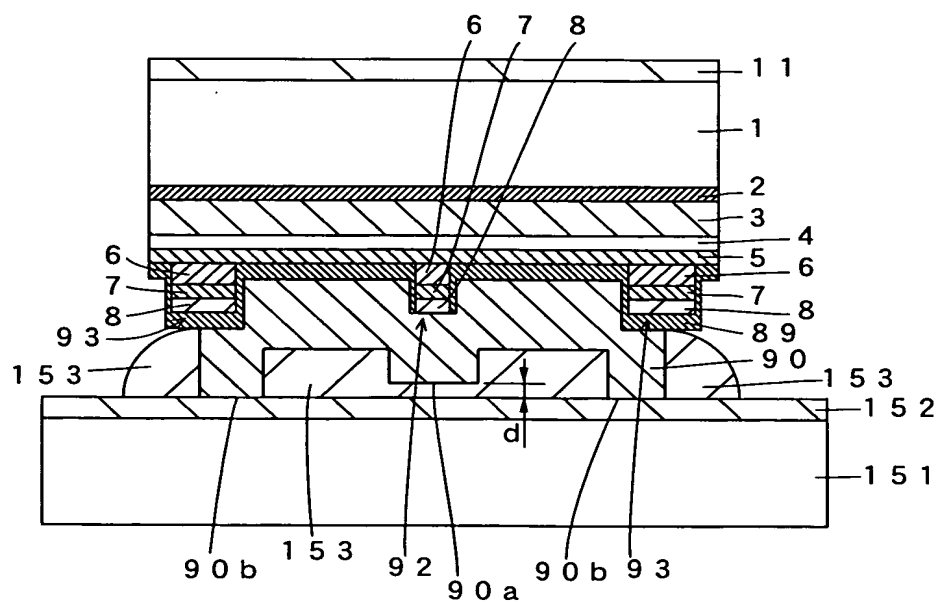


FIG.40

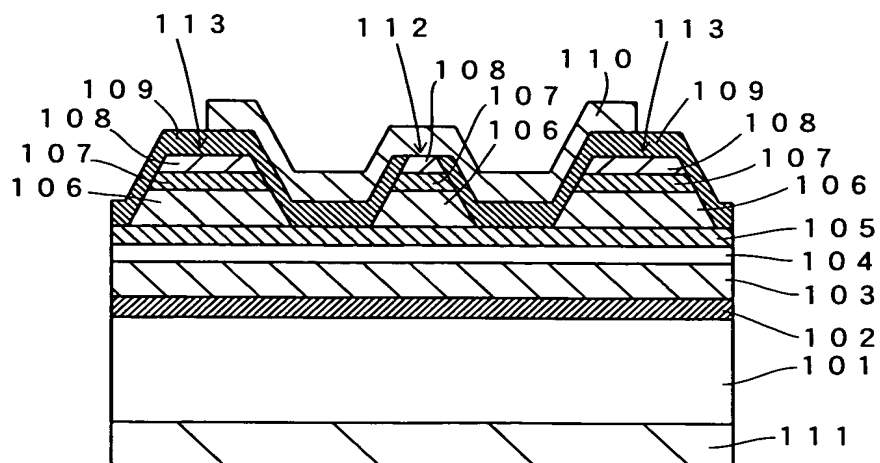


FIG.41

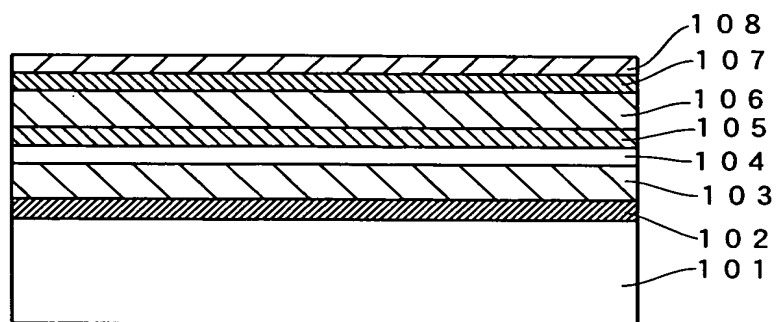


FIG.42

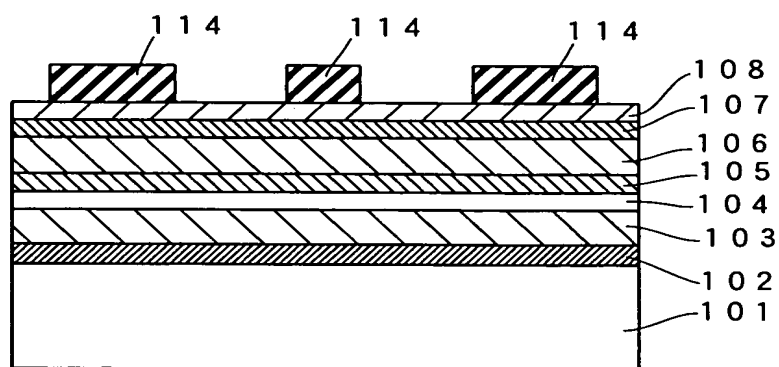


FIG.43

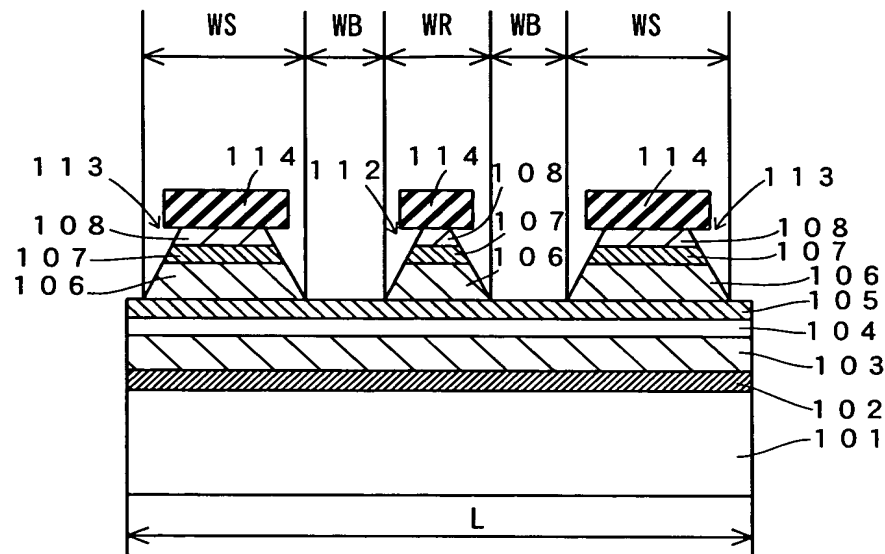


FIG.44

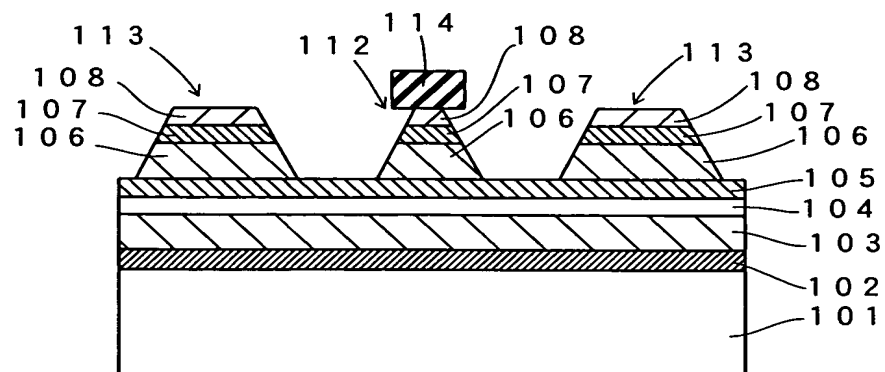


FIG.45

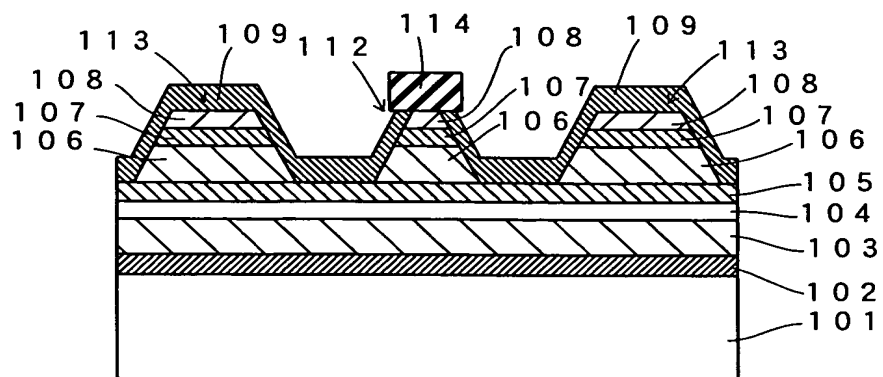


FIG.46

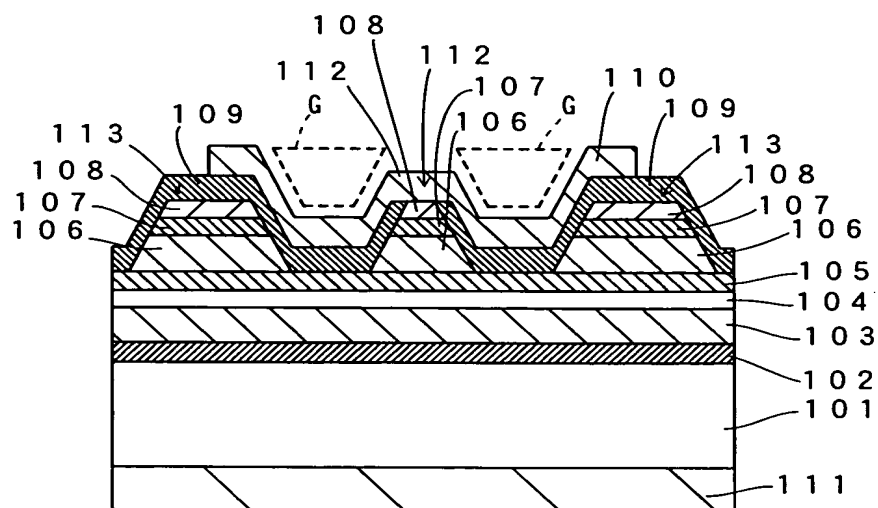


FIG.47

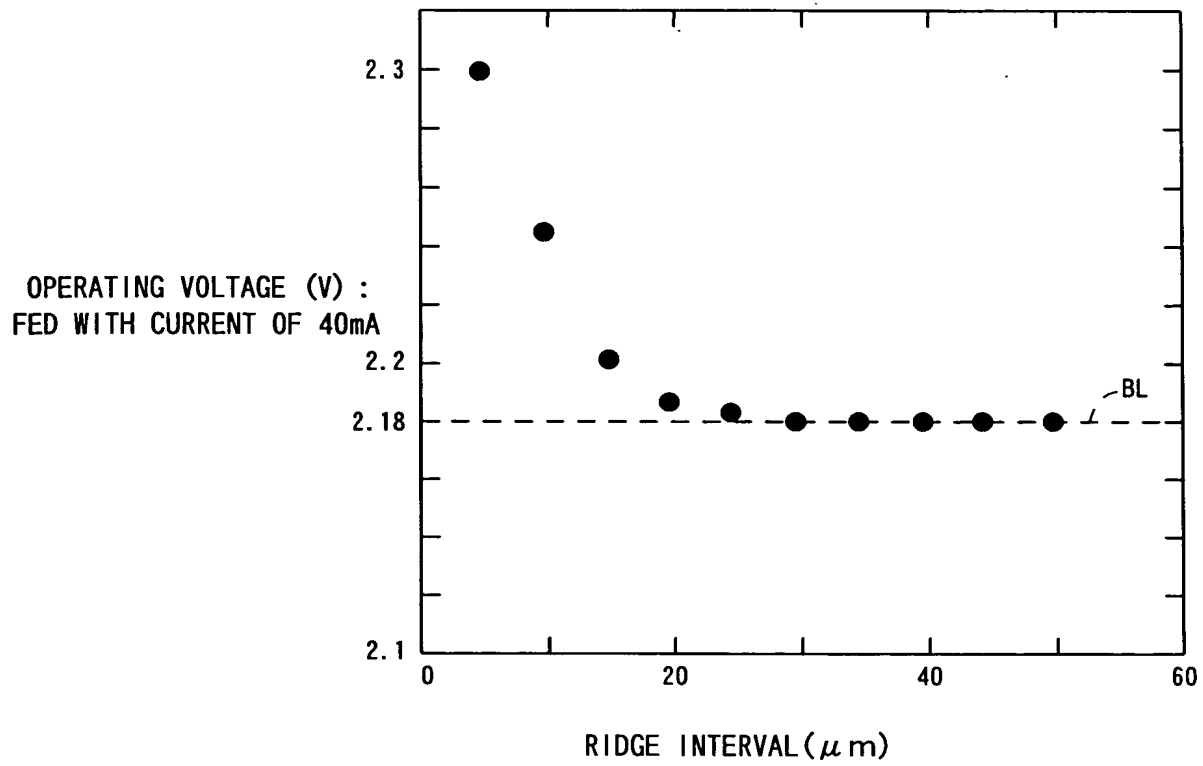


FIG.48

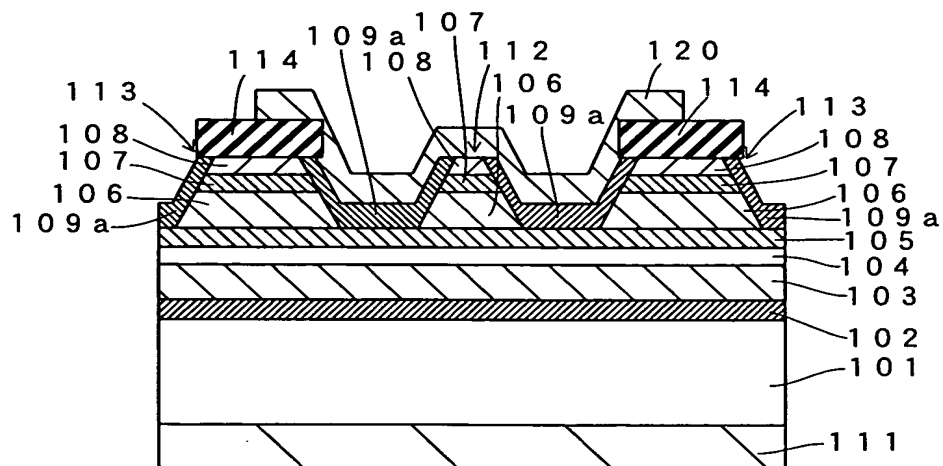


FIG.49

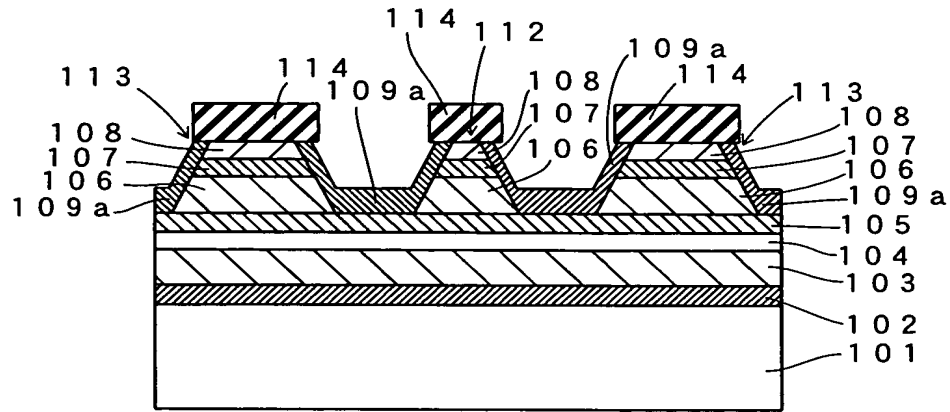


FIG.50 PRIOR ART

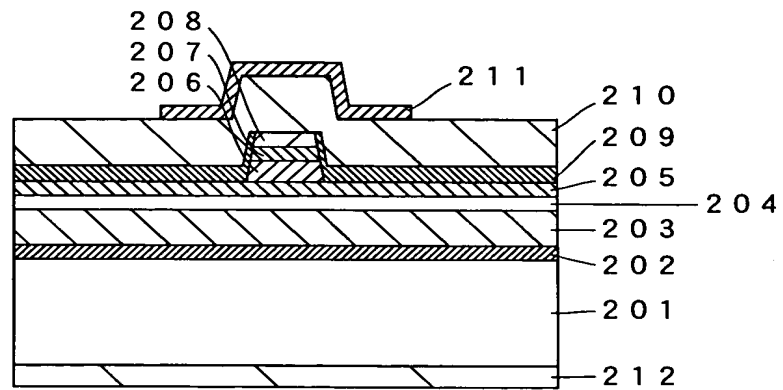


FIG.51 PRIOR ART

